## REMARKS

The Final Office Action mailed January 28, 2004, has been received and reviewed. Claims 6 through 10, 18, 19, 22, 23, 25, and 26 are currently pending in the application. Claims 6 through 10, 18, 19, 22, 23, 25, and 26 stand rejected. Applicants have not amended any claims herein, and respectfully request reconsideration of the application as proposed herein.

**Supplemental Amendment**

Applicants' undersigned attorney notes the filing herein of a Supplemental Amendment on October 27, 2003, which filing was not acknowledged in the outstanding Office Action. Should the Supplemental Amendment have failed for some reason to have been entered in the Office file, Applicants' undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

**35 U.S.C. § 103(a) Obviousness Rejections**

Obviousness Rejection Based on U.S. Patent No. 5,838,038 to Takashima et al. in View of U.S. Patent No. 5,610,418 to Eimori; U.S. Patent No. 5,654,577 to Nakamura et al.; and U.S. Patent No. 5,287,000 to Takahashi et al.

Claims 6 through 10, 18, 19, 22, 23, 25 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takashima et al. (U.S. Patent No. 5,838,038) in view of Eimori (U.S. Patent No. 5,610,418); Nakamura et al. (U.S. Patent No. 5,654,577); and Takahashi et al. (U.S. Patent No. 5,287,000). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable

> expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 6 through 10, 18, 19, 22, 23, 25 and 26 are improper because, at the very least, the cited prior art does not teach or suggest all the claim limitations in sufficient detail that would enable a combination of the references to result in any operable combination to establish a prima facie case of obviousness regarding the claimed invention.

The Examiner's proposed combination of "a DRAM of cell size of $2Fx3F=6F^2$" of Takashima ('038) (col. 25, lines 17-18) with a design rule of adequate reduction, such as a 0.25 micron design rule from Eimori is improper. Specifically, while Takashima discloses that "a DRAM of cell size of $2Fx3F=6F^2$ in which random access can be made and noise is small and which has trench capacitor type memory cells can be realized" (col. 25, lines 17-20), there is no disclosure of any specific design rule for allowing any specific memory cell densities. Therefore, the Examiner has derived a specific design rule, namely 0.25 microns, as a design rule that would result in densities in accordance with those of the claimed invention. However, Eimori nor Takashima, either individually or in any proper combination, disclose how to make a $6F^2$ memory cell using the design rule of 0.25 microns since the problems and solutions associated with shrinking Takashima's $6F^2$ memory cell are not disclosed.

In response to Applicants' previous arguments, the Office Action states, "Applicant states that the references cannot be combined and do not show the claimed device but as described above, Eimore shows that a specific feature size can be realized and since the features size is not shown by Takahashi et al it would be obvious to use Eimore to size the device." (Office Action p. 4).

Applicants respectfully disagree. The substitution that the Office Action proposes as being obvious is a considerable oversimplification of semiconductor process technology. The Office Action states that

> "Takashima et al ('038) shows . . . a DRAM device where the cell size is $6F^2$ (column 25, line 17) but does not show a minimum feature size, peripheral circuitry, array size or packaging. Eimore shows (see cover figure and column 8, line 9) a DRAM (column 1,

> line 9) where a 0.25 micron design rule is used (column 10, line 61) . . [i]t would have been obvious to include the peripheral circuitry show by Nakamura et al. since it provides a working device, to include the feature size shown by Eimore since it is know to be functional and to provide a 16M device since it is known to be useful. Note that with the 0.25 micron design rule the area of the memory is less than 6 $mm^2$. (Office Action p. 2).

The Office Action errs in assuming that processes may simply be substituted at will into various designs. Applicants reiterate that Takashima does not even hint at disclosing the technology to implement the dimensions as proposed nor is there any hint at how such a combination could be integrated. In order to implement an enabling embodiment of the present technology, significant attention must be paid to lines and pitches and spaces which affect essentially all aspects of the design, including active areas, spaces, pitches polysilicon and metal layers. It doesn't necessarily follow that one can apply an $8F^2$ technology to a $6F^2$ design. (Applicants note that currently, only the assignee of record has memory devices in production that utilize $6F^2$ design as the implementation of such is not elementary nor is the substitution of such design specifications.)

Applicants respectfully disagree with the Office Actions' statement that "Note that with the 0.25 micron design rule the area of theory is less than 6 $mm^2$." Applicants respectfully assert that 0.25 is a minimum feature size is NOT the only factor for calculating the array size. The array size is based upon pitch as well. Therefore, while features may approach 0.25 microns, the companion features are on the order of 0.35 microns or larger. Therefore the array size is actually calculated base upon row and column pitches which dictate the cell size, and not the minimum feature size. Specifically, in reference to Eimori, and to a memory cell as illustrated in FIG. 6 of Eimori, even though the illustrated design may be considered "0.25 micron" because the smallest feature size is 0.25 micron, the dimensions illustrate that the pitch is actually 0.35 micron and what is actually being printed is 0.25 and 0.35 microns. Therefore, the array size is much larger and is not the $6mm^2$ as alleged by the Office Action.

Regarding the Takashima ('038) patent, Takashima does not discuss specific dimensions of semiconductor devices. Application of a process such as Eimori to Takashima would require significant process changes or at least significant experimentation, if at all possible.

As disclosed in Applicants' specification, shrinkage of the memory cell, whether $8F^2$ or $6F^2$, to reach a 0.6 micron memory cell pitch involves a number of significant problems.

(Applicants' specification p. 2, line 19). As one example, as the minimum pitch falls below 1.0 micron, conventional "LOCal Oxidation of exposed Silicon" (LOCOS) techniques fail due to excessive encroachment of the oxide beneath the masking stack. (Applicants' specification p. 7, lines 13-16). Furthermore, the memory cell storage node capacitance tends to decrease with the decrease in cell size, yet a minimum storage capacity for stored charge is required to maintain reliable operation. (Applicants' specification p. 8, lines 5-7). As yet another example of scaling issues, adequate spacing is required between adjacent devices, such as between a bit line contact and construction of a capacitor. (Applicants' specification p. 20, lines 3-6). Furthermore, field oxide regions, such as field oxide that is used to provide electrical isolation between certain adjacent banks of memory cells within an array, need to be eliminated to reduce size. (Applicants' specification p. 26, lines 7-11).

Additionally, bit line circuitry and bit line spacing affect the feasibility of shrinking an individual memory cell design within an array to a $6F^2$ size. (Applicants' specification p. 27, line 23 to p. 28, line 1). Furthermore, the space consumed by the digit lines D and D* and their associated circuitry become one of the limiting factors for conversion to a $6F^2$ size. (Applicants' specification p. 28, lines 15-17). All of the aforementioned design considerations would need to be addressed in order for the memory cell as disclosed by Takashima to be shrunk to a 0.6um memory cell resulting in the densities as claimed by Applicants in independent claim 6. As a further example, the memory cell of Takashima as illustrated in Figure 28, includes LOCOS isolation, illustrated as oxide 133 under the word lines and between adjacent memory cells, with spacing also illustrated between bit line contacts and storage nodes. A simple reduction in the photolithographic feature size would result in the problems that are identified and addressed only by Applicants' invention as claimed.

Therefore, Applicants' respectfully request that the rejection of independent claims 6, 18 and 22 and claims 7-10, 19, 23, 25 and 26 depending therefrom be withdrawn. Applicants submit that claims 6 through 10, 18, 19, 22, 23, 25 and 26 are clearly allowable over the cited prior art.

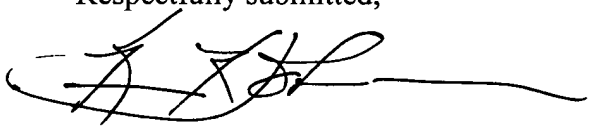
Applicants request the allowance of claims 6 through 10, 18, 19, 22, 23, 25 and 26 and the case passed for issue. Applicants request entry of this amendment for the following reasons:

The amendment is timely filed.
The amendment places the application in condition for allowance.
The amendment does not require any further search or consideration as no claim has been amended.
The amendment narrows the issues of any subsequent appeal of the Final Rejection.

## CONCLUSION

Claims 6 through 10, 18, 19, 22, 23, 25, and 26 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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